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HARDWARE MANUAL



COMPEX SYSTEMS

WP18 BareBoard
WP18 BareBoard
WP18 BareBoard
WP18 BareBoard

Revision: 1.2



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REVISION HISTORY

Revision	Information / Changes
Rev 1.1	First release for WP18 BareBoard
Rev 1.2	Added Support for Open-WRT

REASONS USING DEVELOPMENT KIT

The Development Kit is especially useful for customers who are developing their firmware. Below are the reasons how we have made it more user-friendly for you.

PURPOSE	WHY IS DEVELOPMENT KIT USEFUL?
Develop Redboot/Snapgear OR Open-WRT on WP18	Serial Converter can be used to debug the Open-WRT firmware.
Port Own Firmware Over to WP18	Serial Converter can be used to debug the Serial Output messages.
Port Own Firmware and Loader Over to WP18	Serial Converter can be used to debug the Serial Output messages. JTAG Programmer can be used to load in your loader.

Ordering Options - Standard Configurations*

ORDER CODE	CONTENTS
P-S4 OEMWP181A P-S4 OEMWP186A (For RoHS)	<ul style="list-style-type: none"> • WP18 IXP422 (266MHz CPU) Bare-board (Pre-loaded with CompeX Firmware) • Bareboard embedded with 32MB SDRAM / 4MB Flash
P-S4 OEMWP183B P-S4 OEMWP186B (For RoHS)	<ul style="list-style-type: none"> • WP18 IXP425 (533MHz CPU) Bare-board (Pre-loaded with CompeX Firmware) • Bareboard embedded with 64MB SDRAM / 8MB Flash
WP18 3B DEV KIT WP18 6B DEV KIT (For RoHS on WP18 Bareboard)	<ul style="list-style-type: none"> • WP18 IXP425 (533MHz CPU) Bare-board (Pre-loaded with CompeX Firmware) • Bareboard embedded with 64MB SDRAM/8MB Flash • Wireless G mini-PCI (CompeX WLM54G) • Wireless AG mini-PCI (CompeX WLM54AG) • PoE+ Injector (CompeX PoE+1A4815) • JTAG Programmer (Cable from PC to JTAG Programmer included) • Serial Converter (Cable from PC to Serial Converter included) • 5V DC Adapter

* Configurations are subjected to change without notice

CONFIGURATION AND INSTALLATION

The following is the GPIO Bit mapping specific to the Complex WP18.

GPIO Bit Mapping

The Complex WP18 GPIO bit mapping is shown below.

GPIO Bit	Description
0	Software Push Button
1	CPLD
2	CPLD
3	Uart DCD (not used)
4	Uart RI (not used)
5	Uart DSR (not used)
6	Uart DTR (not used)
7	Software reset
8	Not used
9	Not used
10	PCI INT B
11	PCI INT A
12	CPCI_RST_N
13	CPLD
14	PCI CLOCK
15	Ext Bus Clock

Interface Connectors

The Complex WP18 Bareboard interface connector pin assignments and signal descriptions are included in the following sections. The connectors are listed in the section below and the connector locations are shown in the following diagrams.

<u>Connector</u>	<u>Function</u>
J1	Power Jack DC 5V
J2	Xilinx Port
J4	COM1 Serial Port Header
J6	JTAG Port Header
JP01	POE power and Power Jack selection
TP3	Four LAN port Ethernet connector
U12	One WAN port Ethernet connector
P5	9 pin Serial port

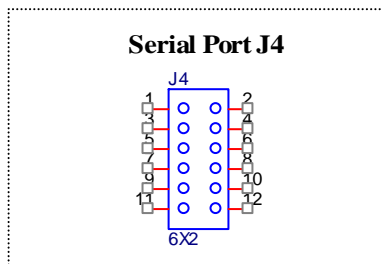
Serial Port Header

The Compex WP18 Bareboard Serial Port (J4) Header signaling is shown in the following table. This serial port uses TTL signals, and therefore you have to use serial converter using MAX-232 IC (or other IC in the market that convert TTL signals to RS232 signals) in order to use it with the PC.

Please take note that Compex Redboot/Snapgear does not run from this Serial Port. Compex RedBoot/Snapgear runs from the 9 Pin Serial Port (P5). Open-WRT is able to run from this port.

<u>Pin</u>	<u>Signal</u>	<u>Pin</u>	<u>Signal</u>
1	5V	2	3.3V
3	5V	4	3.3V
5	Not used	6	TXD
7	Not used	8	RXD
9	GND	10	RTS
11	GND	12	CTS

Note: Our Serial port Implementation requires an external high-impedance serial port not usually available with the serial ports of the notebooks/computers. You will need a Serial Converter available in the market. For our customers' convenience, it is available from Compex, bundled together with the Compex WP18 RedBoot/Snapgear Development Kit.



9 Pin Serial Port

The 9 Pin Serial Port (P5) is used to run the RedBoot/Snapgear from Complex. It uses a Cross Cable.

Serial Console Settings

The serial console settings used together with the serial ports (J4 and P5) is given below.

Baud Rate	115200
Data	8 Bit
Parity	None
Stop	1 Bit
Flow Control	None

JTAG Port Header

The primary purpose of the Complex WP18 Bareboard JTAG Port Header is to facilitate program download into Flash memory.

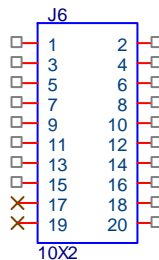
<u>Pin</u>	<u>Signal</u>	<u>Pin</u>	<u>Signal</u>
1	3.3V	2	3.3V
3	TRST_N	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	GND	12	GND
13	TDO	14	GND
15	SRST_N	16	GND
17	Empty	18	GND
19	Empty	20	GND

Note:

Complex has a JTAG Programmer compatible with WP18 Bareboard. It is bundled with Complex WP18 Development Kit. This JTAG programmer is able to download file onto the Flash, and thus recover a corrupted loader.



JTAG Connector



Ethernet Connectors

The CompeX WP18 Bareboard contains 2 X 10/100 Base-TX Ethernet Channels. Both Ethernet Channels are available through standard 8-pin RJ45 connectors. The U10 and U12 Ethernet Connectors both support Active Power-Over-Ethernet.

Ethernet Connectors signaling is shown below.

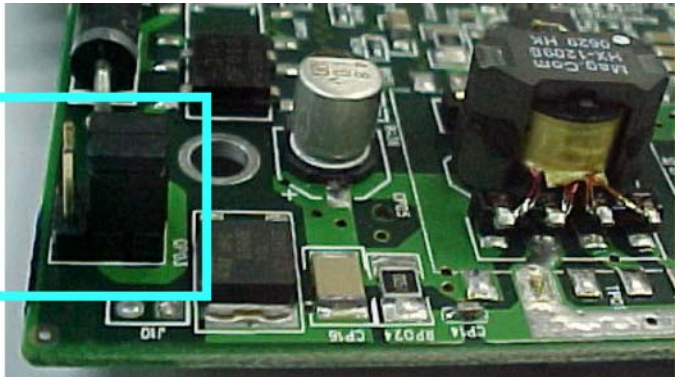
<u>Pin</u>	<u>Signal</u>
1	TX+
2	TX-
3	RX+
4	PoE+V
5	PoE+V
6	RX-
7	GND
8	GND

Ethernet Connector U10 or U12

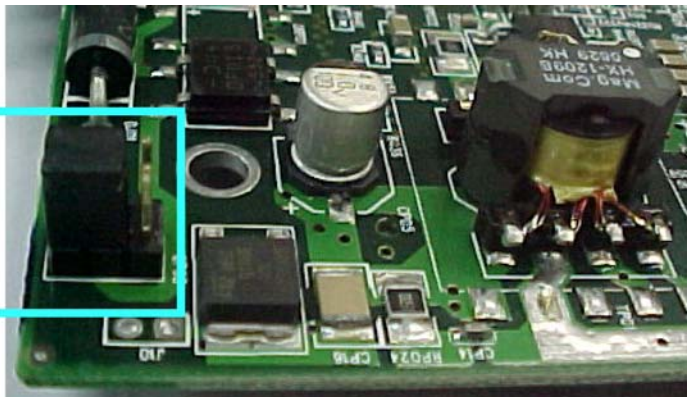
Power Jumper Connector

CompeX WP18 Bareboard supports both Active PoE and DC Jack. To support either Active PoE or DC Jack, please set the jumpers on JP01 as shown below:

Active PoE
Jumper Selection



DC Jack
Jumper Selection



Additional Notes

1. A Software Development Kit for porting over your source codes is available. Please contact a Complex salesperson for details.

Additional Notes (For RedBoot/Snapgear)

1. Default IP address for WP18 Bareboard 192.168.0.254
2. Default Server IP address is 192.168.0.1
3. MAC Address is default.
We are in the process of making the RedBoot/Snapgear a Complex MAC address. (For RedBoot/Snapgear)
4. RedBoot boards come preloaded with the RedBoot Loader and Snapgear.

Additional Notes (For Open-WRT)

1. Our Open-WRT is based on the current development branch, Kamikaze.
2. Please download Open-WRT Source Codes from http://complex.com.sg/home/OEM/Open_wrt.htm
3. The Open-WRT is based on Linux 2.6. The Open-WRT will run off the Complex loader originally on the board.
4. Default IP address for
LAN Port: 192.168.1.1
Wan Ports is: 192.168.0.2
5. MAC Address is Complex MAC Address (00-80-48-XX-XX-XX).
6. For uploading Open-WRT Source Code, Please refer to the "Read ME WP18.txt" in
 - a. ../WP18(Open-WRT)/WP18 4MB/ For 4MB flash or
 - b. ../WP18(Open-WRT)/WP18 8MB/ For 8 MB flash.

7. Flash Memory Map:

Offset:

0x00000000	Compex Loader
0x00080000	Linux Kernel
0x00300000	JFFS, Root FS
0x003E0000(4MB) 0x007E0000(8MB)	Redboot fis, Redboot config

8. Is there any space available for the JFFS partition?

The JFFS partition is fixed. It is between (0x003000000 - 0x003E0000(4 Or 007E0000(8MB))

9. What can be the maximum size for TRX?

The maximum size for TRX is (0x3F0000 – 0x50000) = 3801088 bytes. If the TRX reaches maximum size, there is no JFFS partition

10. What is the use of the JFFS partition? Can we store configuration files if there is no JFFS partition?

Our current Open-WRT stores configuration files in writable JFFS partition. Configuration cannot be saved if there is no JFFS partition, although it can still run using default configurations.

11. Please do note that ONLY when Compex Loader is V2.40 and above, then it can support the use of Open-WRT.